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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/529,049	03/24/2005	Ronald Kakoschke	10808/227	1781
7590 Brinks Hofer Gilson & Lione P O Box 10395 Chicago, IL 60610				
09/03/2008				
EXAMINER				
SALERNO, SARAH KATE				
ART UNIT		PAPER NUMBER		
2814				
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09/03/2008		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

ADVISORY ACTION (continuation of page 1)

The request for reconsideration has been considered but the amendment will not be entered for the following reasons:

New issues corresponding to new claim limitations (An integrated field-effect transistor, having a substrate region surrounded: by two terminal regions, one terminal region being a source region and the other terminal region being a drain region, the Source region being arranged at first side of the substrate region and the drain region being arranged at a second side of the substrate region, the first and second sides being opposite sides of the substrate region; by two electrically insulating insulating layers, which are arranged at a third and fourth side of the substrate region, the third and fourth sides being mutually opposite sides of the substrate region and the insulating layers being ^{[[are]]} adjoined by control regions, the first and second sides being narrower than the third and fourth sides; by two electrically insulating regions, the insulating regions being arranged at mutually opposite sides of the substrate region, and by an electrically conductive connecting region or a part of an electrically conductive connecting region which produces an electrically conductive connection between one of the terminal regions and the substrate region, the connecting region comprising a metal-semiconductor compound, part of a covering area of the substrate region being covered by the connecting region, the connecting region also covering a covering area of the source region such that the connecting region extends, across the first side of the

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substrate region to the source region, the part of the covering area of the substrate region covering the substrate region between the insulating layers and between the control regions.) in claim 1 has been added that would require further consideration and/or search.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sarah K. Harding whose telephone number is (571) 270-1266. The examiner can normally be reached on M-R 7:30-5:00pm every other F 7:30-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sarah K Salerno/
Examiner, Art Unit 2814

/Theresa T. Doan/
Primary Examiner, Art Unit 2814